REMARKS

The Office Action of March 23, 2006 has been carefully studied.

Applicants note the indication of claims 14, 16-18 and 22 containing allowable subject matter.

Applicants have amended claim 14 (lines 27 and 32), claim 20 (lines 12 and 17), claim 22 (line 8), and claim 24 (line 18), as suggested in paragraph 1, page 2 of the Office Action. Concerning the comments about "can flow" in claim 7 (line 4) and claim 24 (line 20), the use of the word "can" is correct. The words "can flow" should not be changed to – flows – because at the time the circuit of claims 7 and 24 is sold, current does not flow. It is important for apparatus claims to define subject matter that is infringed at the time the goods are sold, prior to being put into use. The Examiner is requested to provide a case citation to support his position that "can flow" should be changed to – flows –, bearing in mind that the test to determine if a claim complies with 35 U.SC. §112, second paragraph, is whether a member of the public can determine if an existing or planned product infringes the claim. Claim 11, lines 3 and 4, have been amended as suggested.

The present amendment overcomes the rejection of claims 11, 12 and 24-36 under 35 U.S.C. 112, second paragraph. Applicants submit new claims 27-29 that define their contribution to the art in a manner not disclosed by the art of record.

Applicants traverse the anticipation rejection of claims 1, 3, 7 and 8 based on Love, U.S. Patent 5,068,553. The Office Action incorrectly alleges Love discloses pulse shaping circuitry for preventing both source drain paths of field effect transistors 86 and 88 from

being on simultaneously. It is well known that inverters of the type illustrated by inverter 90 of Love have a short circuit current simultaneously flowing through both the NFET and the PFET in response to the NFET and PFET transitioning between the on and off states thereof. In this regard, pages 172-190, Chapter 6, and a portion of Chapter 12 of Kang et al., CMOS Digital Integrated Circuits Analysis and Design (all of which are enclosed as Applicants' Exhibit 1) indicate such a short circuit current simultaneously flows through the NFET and PFET of inverters of the type disclosed by inverter 90 of Love. Figure 5.17, on page 175, and the description thereof indicate inverter 90 of Love (see Figure 5,16 on page 173 of Kang et al.), both the PFET and NFET are in saturation for a considerable range of input voltages at the common gates of the NFET and PFET. Kang et al. discusses this situation, for example, on page 189 in the section entitled "Power and Area Considerations," where it is stated:

> In many applications requiring a low overall power consumption, CMOS is preferred over other circuit alternatives for this reason. It must be noted, however, that the CMOS inverter does conduct a significant amount of current during a *switching* event, i.e., when the output voltage changes from a low state to a high state, or from a high state to a low state.

The power dissipation occurring as a result of switching and such CMOS type inverters is also discussed in detail in section 6.7, pages 243-245 of Kang et al., and pages 456-460 of Kang et al. The first two sentences of the second full paragraph on page 245 state:

> Note that under realistic conditions, when the input voltage waveform deviates from ideal step input and has non-zero rise and fall times, for example, both the nMOS and the pMOS transistor will simultaneously conduct a certain amount of current during the switching event. This is called a short circuit current, since in this case, two transistors temporarily form a conducting path between V_{DD} and the ground.

While the Love circuit differs somewhat from the inverter disclosed by the Kang et al. reference, because of the connection of NFET device 80 as a capacitor between the gates of PFET 86 and NFET 88 and ground, the NFET device does not prevent simultaneous flow of current through the source drain paths of PFET 86 and NFET 88. During a negative going transition of the voltage V_{IN}, capacitor 80 is switched off, as indicated by waveforms 102 and V_{76} in Figures 5a and 5b of Love; if capacitor 80 were switched on during most of the negative going transition of V_{IN}, waveforms 102 and V_{76} would start substantially simultaneously with the beginning of the negative going transitions of V_{IN}. Because capacitor 80 is switched off during the vast majority of the negative going transition of V_{IN} from the power supply voltage to ground, the transition is coupled without any substantial delay to the gates of both PFET 86 and NFET 88. Consequently, both PFET 86 and NFET 88 are simultaneously on during the transition as described by Kang et al. Dependent claims 3, 7 and 8 are allowable for the same reasons advanced for claim 1, upon which claims 3, 7 and 8 depend.

Applicants traverse the rejection of claims 1, 3, 7-12, 20, 21 and 23-26 as being unpatentable over Bui et al., U.S. Patent 6,201,752, in view of Wanlass, U.S. Patent 3,356,858. Independent claims 1 and 24 distinguish over the proposed combination by requiring pulse shaping circuit type presenting both source drain paths from being on simultaneously.

The Office Action proposes to employ an inverter, such as disclosed by Wanlass, as inverter 809 of Bui et al. The Wanlass inverter suffers from the same problems as the Love inverter, as indicated by the Kang et al. book. As a result, the Wanlass inverter does not meet the requirement of claim 1 or claim 24 for pulse shaping circuitry for preventing

both source drain paths from being on simultaneously. The connections of capacitive elements 807 and 808 to the input terminal of inverter 809 do not prevent the type of operation disclosed by Kang et al. from occurring in the Wanlass inverter. This is because the gate electrodes of the Wanlass field effect transistors are driven in parallel by the voltage on lead 804. Consequently, the same voltage is applied to the gate electrodes of both transistors in the Wanlass inverter, thereby causing the simultaneous presence of current flow through the Wanlass transistors, despite the delay characteristics associated with capacitive elements 807 and 808.

Independent claim 20, as amended, distinguishes over the proposed combination of Bui et al. and Wanlass by requiring the source drain path the second transistor, i.e., one of the transistors of the inverter of the pulse shaping circuitry, to be connected directly between the output terminal of the inverter and one of the power supply terminals so that the voltage at the one power supply terminals is always applied directly to the output terminal of the inverter by the source drain path of second transistor while the source drain path of the second transistor is switched on. In Bui et al., the inverter including PFET 802 and NFET 806 includes resistors 803 and 804. Current flows through resistor 803 while PFET 802 is switched on. Current flows through resistor 805 while transistor 806 is switched on. Consequently, the foregoing limitation of claim 20 is not found in the applied art.

Dependent claims 3, 7-12, 21, 23, 25 and 26 are allowable for the same reasons advanced for the claims upon which they depend. In addition, claim 12, as amended, requires the source drain path of the another PFET of the inverter to be connected directly between the output terminal of the inverter and one of the power supply terminals so that

the voltage at the one power supply terminal is always applied directly to the output terminal of the inverter via the source drain path of the another PFET of the inverter while the source drain path of the another PFET of the inverter is switched on. Dependent claim 25 is similar to claim 12, but refers to the NFET of the inverter, instead of the PFET of the inverter.

New claim 27 depends on claim 1, and is allowable therewith. In addition, new claim 27 requires the voltage source to have transitions in both directions between the first and second levels. The pulse shaping circuit is arranged for preventing both source drain paths from being on in response to the transitions in both directions. There is no art of record describing such operation in the circuit of claim 1.

New claim 28 distinguishes over the art of record by requiring a first resistive element to be connected to be responsive to the voltage at a first signal terminal for directly supplying current to a first capacitor and the gate electrode of a first transistor, without directly supplying current to the gate electrode of another of the transistors, wherein the transistors are a PFET transistor and an NFET transistor having source drain paths connected in series between first and second opposite DC power supply terminals. The capacitor is required to be a FET device having a conductivity type opposite that of the first of the transistors. The FET device is required to include first and second electrodes connected between the gate electrodes of the first of the transistors and the power supply terminal for supplying current directly to the source drain path of the second of the transistors.

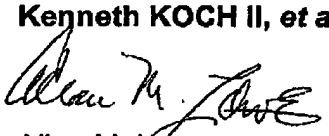
New claim 29 depends on claim 28, and is allowable therewith. Claim 29 further distinguishes over the art of record by requiring a second resistive element to be

connected for supplying current to a second capacitor and the gate electrode of an NFET transistor without directly supplying current to the first capacitor and the gate electrode of a PFET transistor that claim 29 indicates is the first transistor of claim 28. In addition, the second capacitor is required to be a PFET device having a first electrode connected between the gate electrode of the NFET transistor and a second electrode connected to the first power supply terminal. The foregoing is not disclosed by the art of record.

In view of the foregoing amendments and remarks, favorable reconsideration and allowance are in order.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025, and please credit any excess fees to such deposit account.

Respectfully submitted,
Kenneth KOCH II, *et al.*



Allan M. Lowe
Registration No. 19,641

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400
Telephone: 703-684-1111
Facsimile: 970-898-0640

Date: June 22, 2006

AML/dll

second edition

CMOS DIGITAL INTEGRATED CIRCUITS

Analysis and Design

SUNG-MO (STEVE) KANG
University of Illinois at Urbana- Champaign

YUSUF LEBLEBICI
Worcester Polytechnic Institute
Swiss Federal Institute of Technology-Lausanne

WCB McGraw-Hill

Boston Burr Ridge, IL Dubuque, IA Madison, WI New York San Francisco St. Louis
Bangkok Bogotá Caracas Lisbon London Madrid
Mexico City Milan New Delhi Seoul Singapore Sydney Taipei Toronto

Exhibit 1

WCB/McGraw-Hill

A Division of The McGraw-Hill Companies

To Myoung-A, Jennifer and Jefferey, and Anil and Ebru

CMOS DIGITAL INTEGRATED CIRCUITS: ANALYSIS AND DESIGN

This book is printed on acid-free paper.

1 2 3 4 5 6 7 8 9 0 DOC/DOC 9 9 2 1 0 9 8

ISBN 0-07-292507-8

Vice president and editorial director: Kevin T. Kane
Publisher: Thomas Casson
Executive editor: Elizabeth A. Jones
Senior developmental editor: Kelley Butcher
Marketing manager: John T. Wannemacher
Project manager: Karen Nelson
Senior production supervisor: Heather D. Burbridge
Senior designer: Loma Lo
Cover designer: Nicole Leong
Supplement coordinator: Linda Huenecke
Typeface: 10/12 Times Roman
Printer: R. R. Donnelley & Sons Company

Library of Congress Cataloging-in-Publication Data

Kang, Sung Mo, (date)
CMOS digital integrated circuits: analysis and design/Sung-Mo (Steve) Kang, Yusuf Leblebici.
–2nd ed.
p. cm.
Includes index.
ISBN 0-07-292507-8
1. Metal oxide semiconductors, Complementary. 2. Digital integrated circuits. I. Leblebici, Yusuf.
II. Title.
TK7871.99M44K36 1999
621.39'5–dc21

98-28075

http://www.mhhe.com

Next, substitute V_{out} in the KCL equation (5.42), to obtain

$$2\cdot\left[2\cdot(V_{IH}-1)\cdot(0.5\,V_{IH}-0.55)-(0.5\,V_{IH}-0.55)^2\right]=\frac{1}{3}\cdot(2.95)^2$$

The solution of this simple quadratic equation yields two values for V_{IH}:

$$V_{IH}=\begin{cases}-0.35\ \text{V}\\ \underline{2.43\ \text{V}}\end{cases}$$

where $V_{IH}=2.43$ V is the physically correct solution. The output voltage level at this point is calculated as

$$V_{out}=0.5\cdot 2.43-0.55=0.67\ \text{V}$$

With this updated output voltage value, we can now reevaluate the load threshold voltage as $V_{T,load}(V_{out}=0.67\ \text{V})=-2.9$ V, and the $(dV_{T,load}/V_{out})$ value as

$$\frac{dV_{T,load}}{dV_{out}}=0.18$$

Note both of these values are fairly close to those used at the beginning of this iteration process. Repeating the iterative calculation will provide only a marginal improvement of accuracy, thus, we may accept $V_{IH}=2.43$ V as a good estimate.

In conclusion, the noise margins for high signal levels and for low signal levels can be found as follows:

$$NM_H=V_{OH}-V_{IH}=2.57\ \text{V}$$
$$NM_L=V_{IL}-V_{OL}=1.17\ \text{V}$$

5.4. CMOS Inverter

All of the inverter circuits considered so far had the general circuit structure shown in Fig. 5.3, consisting of an enhancement-type nMOS driver transistor and a load device which can be a resistor, an enhancement-type nMOS transistor, or a depletion-type nMOS transistor acting as a nonlinear resistor. In this general configuration, the input signal is always applied to the gate of the driver transistor, and the operation of the inverter is controlled primarily by switching the driver. Now, we will turn our attention to a radically different inverter structure, which consists of an enhancement-type nMOS transistor and an enhancement-type pMOS transistor, operating in complementary mode (Fig. 5.16).

This configuration is called Complementary MOS (CMOS). The circuit topology is complementary push-pull in the sense that for high input, the nMOS transistor drives (pulls down) the output node while the pMOS transistor acts as the load, and for low input the pMOS transistor drives (pulls up) the output node while the nMOS transistor acts as the load. Consequently, both devices contribute equally to the circuit operation characteristics.

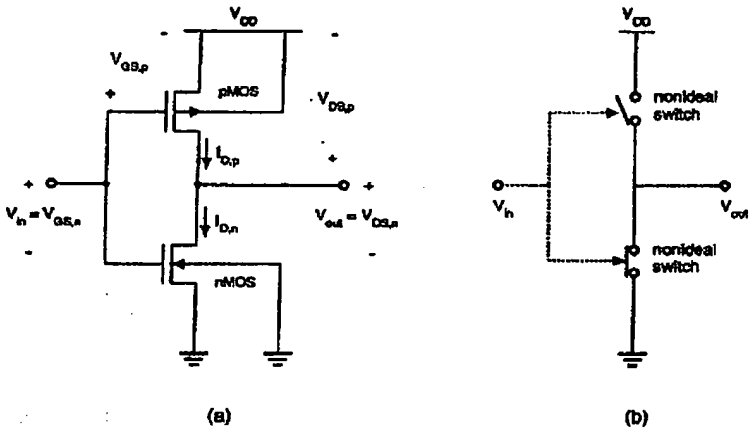


Figure 5.16. (a) CMOS inverter circuit. (b) Simplified view of the CMOS inverter, consisting of two complementary nonideal switches.

The CMOS inverter has two important advantages over the other inverter configurations. The first and perhaps the most important advantage is that the steady-state power dissipation of the CMOS inverter circuit is virtually negligible, except for small power dissipation due to leakage currents. In all other inverter structures examined so far, a nonzero steady-state current is drawn from the power source when the driver transistor is turned on, which results in a significant DC power consumption. The other advantages of the CMOS configuration are that the voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and V_{DD}, and that the VTC transition is usually very sharp. Thus, the VTC of the CMOS inverter resembles that of an ideal inverter.

Since nMOS and pMOS transistors must be fabricated on the same chip side- by-side, the CMOS process is more complex than the standard nMOS-only process. In particular, the CMOS process must provide an n-type substrate for the pMOS transistors and a p-type substrate for the nMOS transistors. This can be achieved by building either n-type *tubs* (wells) on a p-type wafer, or by building p-type tubs on an n-type wafer (cf. Chapter 2). In addition, the close proximity of an nMOS and a pMOS transistor may lead to the formation of two parasitic bipolar transistors, causing a *latch-up* condition. In order to prevent this undesirable effect, additional *guard rings* must be built around the nMOS and the pMOS transistors as well (cf. Chapter 13). The increased process complexity of CMOS fabrication may be considered as the price being paid for the improvements achieved in power consumption and noise margins.

In Fig. 5.16, note that the input voltage is connected to the gate terminals of both the nMOS and the pMOS transistors. Thus, both transistors are driven directly by the input signal, V_{in}. The substrate of the nMOS transistor is connected to the ground, while the substrate of the pMOS transistor is connected to the power supply voltage, V_{DD}, in order to reverse-bias the source and drain junctions. Since $V_{SB} = 0$ for both devices, there will be no substrate-bias effect for either device. It can be seen from the circuit diagram in Fig. 5.16 that

$$V_{GS,n} = V_{in} \qquad V_{DS,n} = V_{out} \tag{5.51}$$

and also,

$$V_{GS,p} = -(V_{DD} - V_{in}) \qquad V_{DS,p} = -(V_{DD} - V_{out}) \tag{5.52}$$

We will start our analysis by considering two simple cases. When the input voltage is smaller than the nMOS threshold voltage, i.e., when $V_{in} < V_{T0,n}$, the nMOS transistor is cut-off. At the same time, the pMOS transistor is on, operating in the linear region. Since the drain currents of both transistors are approximately equal to zero (except for small leakage currents), i.e.,

$$I_{D,n} = I_{D,p} = 0 \tag{5.53}$$

the drain-to-source voltage of the pMOS transistor is also equal to zero, and the output voltage V_{OH} is equal to the power supply voltage.

$$V_{out} = V_{OH} = V_{DD} \tag{5.54}$$

On the other hand, when the input voltage exceeds $(V_{DD} + V_{T0,p})$, the pMOS transistor is turned off. In this case, the nMOS transistor is operating in the linear region, but its drain-to-source voltage is equal to zero because condition (5.53) is satisfied. Consequently, the output voltage of the circuit is

$$V_{out} = V_{OL} = 0 \tag{5.55}$$

Next, we examine the operating modes of the nMOS and the pMOS transistors as functions of the input and output voltages. The nMOS transistor operates in *saturation* if $V_{in} > V_{T0,n}$ *and* if the following condition is satisfied.

$$V_{DS,n} \geq V_{GS,n} - V_{T0,n} \quad \Leftrightarrow \quad V_{out} \geq V_{in} - V_{T0,n} \tag{5.56}$$

The pMOS transistor operates in *saturation* if $V_{in} < (V_{DD} + V_{T0,p})$, *and* if :

$$V_{DS,p} \leq V_{GS,p} - V_{T0,p} \quad \Leftrightarrow \quad V_{out} \leq V_{in} - V_{T0,p} \tag{5.57}$$

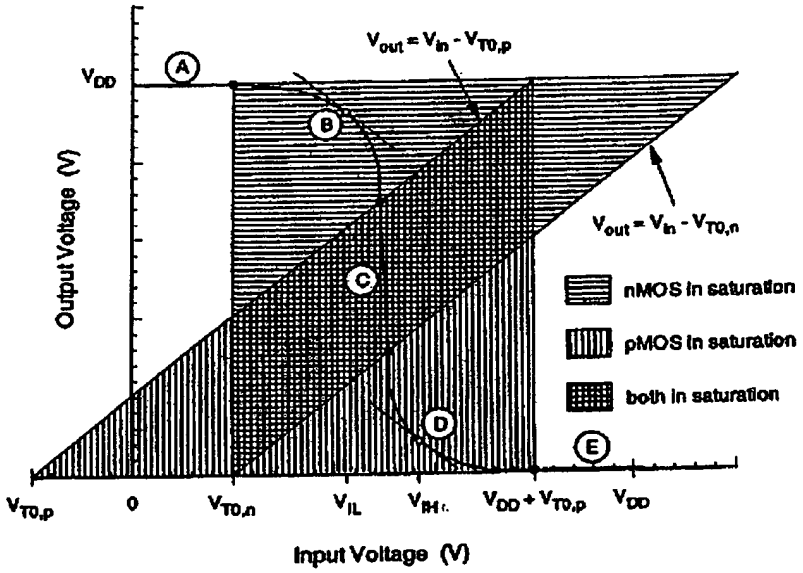


Figure 5.17. **Operating regions of the nMOS and the pMOS transistors.**

Both of these conditions for device saturation are illustrated graphically as shaded areas on the $V_{out} - V_{in}$ plane in Fig. 5.17. A typical CMOS inverter voltage transfer characteristic is also superimposed for easy reference. Here, we identify five distinct regions, labeled A through E, each corresponding to a different set of operating conditions. The table below lists these regions and the corresponding critical input and output voltage levels.

Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$> (V_{DD} + V_{T0,p})$	V_{OL}	linear	cut-off

In Region A, where $V_{in} < V_{T0,n}$, the nMOS transistor is cut-off and the output voltage is equal to $V_{OH} = V_{DD}$. As the input voltage is increased beyond $V_{T0,n}$ (into Region B), the nMOS transistor starts conducting in saturation mode and the output voltage begins to decrease. Also note that the critical voltage V_{IL} which corresponds to $(dV_{out}/dV_{in}) = -1$ is located within Region B. As the output voltage further decreases, the pMOS transistor enters saturation at the boundary of Region C. It is seen from Fig. 5.17 that the inverter threshold voltage, where $V_{in} = V_{out}$, is located in Region C. When the output voltage V_{out} falls below $(V_{in} - V_{T0,n})$, the nMOS transistor starts to operate in linear mode. This corresponds to Region D in Fig. 5.17, where the critical voltage point V_{IH} with $(dV_{out}/dV_{in}) = -1$ is also located. Finally, in Region E, with the input voltage $V_{in} > (V_{DD} + V_{T0,p})$, the pMOS transistor is cut-off, and the output voltage is $V_{OL} = 0$.

In a simplistic analogy, the nMOS and the pMOS transistors can be seen as nearly ideal switches– controlled by the input voltage– that connect the output node to the power supply voltage or to the ground potential, depending on the input voltage level. The qualitative overview of circuit operation, illustrated in Fig. 5.17 and discussed above, also highlights the complementary nature of the CMOS inverter. The most significant feature of this circuit is that the current drawn from the power supply in both of these steady-state operating points, i.e., in Region A and in Region E, is nearly equal to zero. The only current that flows in either case is the very small leakage current of the reverse-biased source and drain junctions. The CMOS inverter can *drive* any load, such as interconnect capacitance or fanout logic gates which are connected to its output node, either by supplying current to the load, or by sinking current from the load.

The steady-state input-output voltage characteristics of the CMOS inverter can be better visualized by considering the interaction of individual nMOS and pMOS transistor characteristics in the current-voltage space. We already know that the drain current $I_{D,n}$ of the nMOS transistor is a function of the voltages $V_{GS,n}$ and $V_{DS,n}$. Hence, the nMOS drain current is also a function of the inverter input and output voltages V_{in} and V_{out}, according to (5.51).

$$I_{D,n} = f(V_{in}, V_{out})$$

This two-variable function, which is essentially described by the current equations (3.54) through (3.56), can be represented as a *surface* in the three-dimensional current-voltage space. Figure 5.18 shows this $I_{D,n}(V_{in}, V_{out})$ surface for the nMOS transistor.

Similarly, the drain current $I_{D,p}$ of the pMOS transistor is also a function of the inverter input and output voltages V_{in} and V_{out}, according to (5.52).

$$I_{D,p} = f(V_{in}, V_{out})$$

This two-variable function, described by the current equations (3.57) through (3.59), can be represented as another surface in the three-dimensional current-voltage space. Figure 5.19 shows the corresponding $I_{D,p}(V_{in}, V_{out})$ surface for the pMOS transistor.

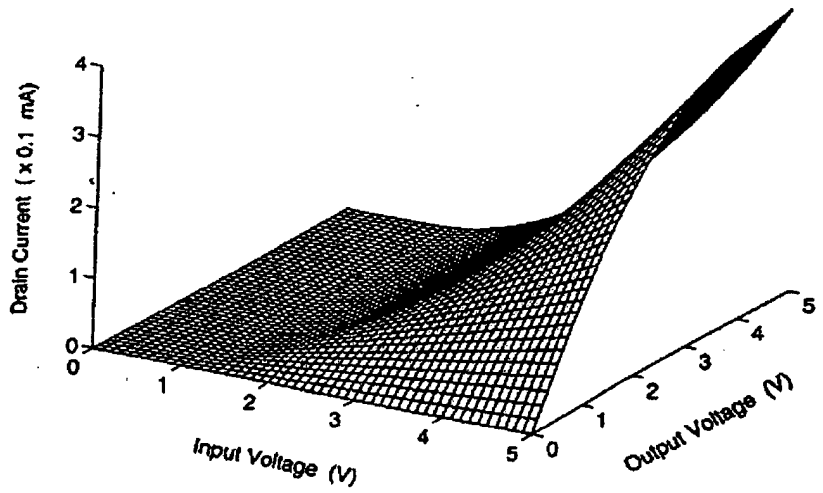


Figure 5.18. Current-voltage surface representing the nMOS transistor characteristics.

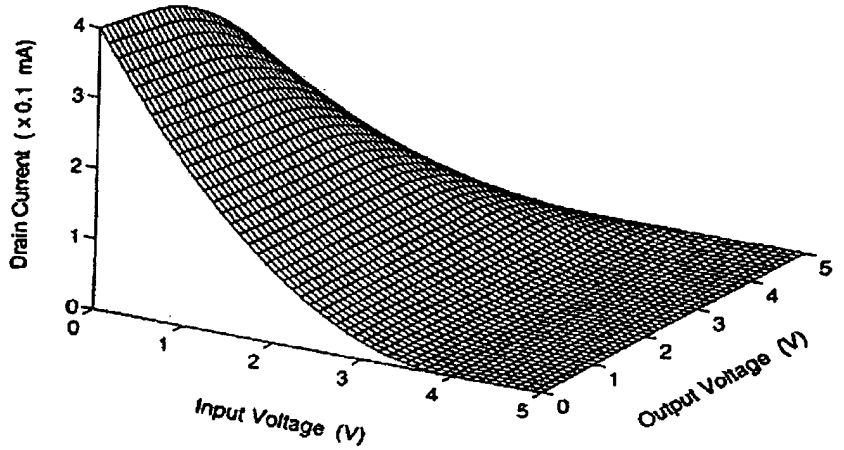


Figure 5.19. Current-voltage surface representing the pMOS transistor characteristics.

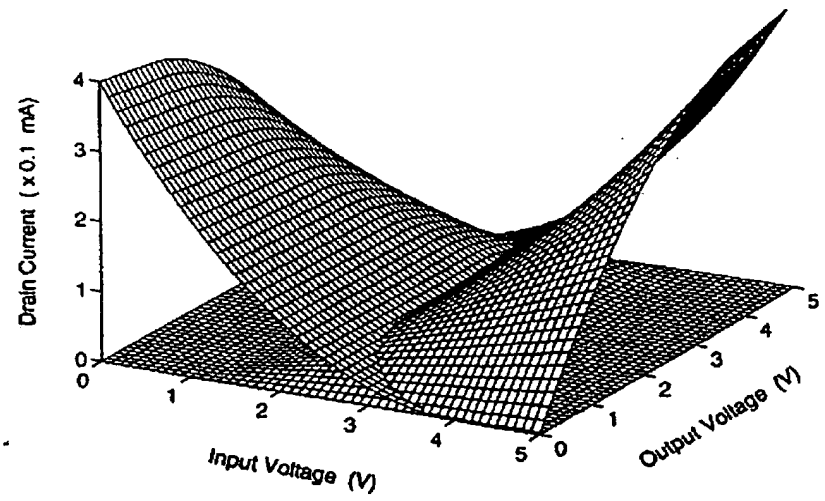


Figure 5.20. Intersection of the current-voltage surfaces shown in Figures 5.18 and 5.19.

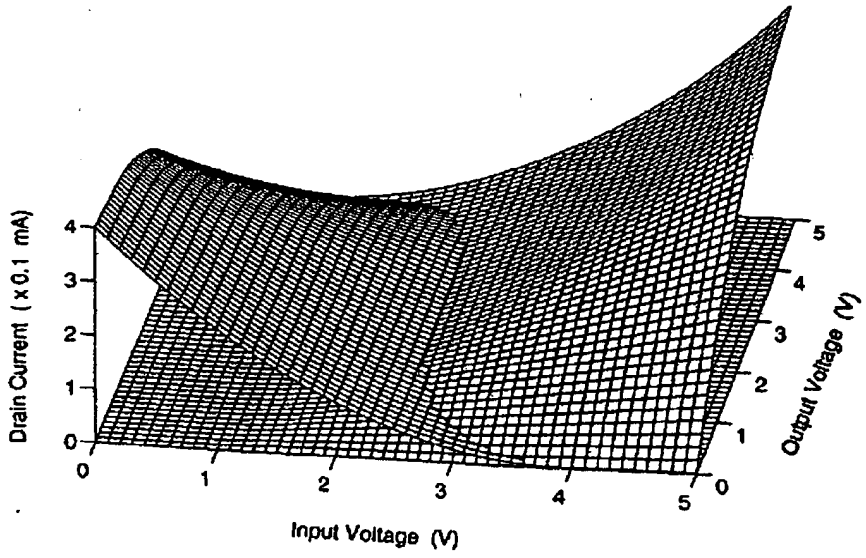


Figure 5.21. The intersecting current-voltage surfaces shown from a different viewing angle. Notice that projection of the intersection curve on the voltage plane gives the VTC.

Remember that in a CMOS inverter operating in steady-state, the drain current of the nMOS transistor is always equal to the drain current of the pMOS transistor, according to KCL.

$$I_{D,n} = I_{D,p}$$

Thus, the *intersection* of the two current-voltage surfaces shown in Figs. 5.18 and 5.19 will give the operating curve of the CMOS inverter circuit in the three-dimensional current-voltage space. The intersection of the two characteristic surfaces is shown in Fig. 5.20. The intersecting surfaces are shown from a different viewing angle in Fig. 5.21, with the intersection curve highlighted in bold.

It is clear that the vertical projection of the intersection curve on the V_{in} - V_{out} plane produces the typical CMOS inverter voltage transfer characteristic already shown in Fig. 5.17. Similarly, the horizontal projection of the intersection curve on the I_D - V_{in} plane gives the steady-state current drawn by the inverter from the power supply voltage as a function of the input voltage. In the following, we will present an in-depth analysis of the CMOS inverter static characteristics, by calculating the critical voltage points on the VTC. It has already been established that $V_{OH} = V_{DD}$ and $V_{OL} = 0$ for this inverter; thus, we will devote our attention to V_{IL}, V_{IH} and the inverter switching threshold, V_{th}.

Calculation of V_{IL}

By definition, the slope of the VTC is equal to (–1), i.e., $dV_{out} / dV_{in} = -1$ when the input voltage is $V_{in} = V_{IL}$. Note that in this case, the nMOS transistor operates in saturation while the pMOS transistor operates in the linear region. From $I_{D,n} = I_{D,p}$, we obtain the following current equation:

$$\frac{k_n}{2}\cdot\left(V_{GS,n} - V_{T0,n}\right)^2 = \frac{k_p}{2}\cdot\left[2\cdot\left(V_{GS,p} - V_{T0,p}\right)\cdot V_{DS,p} - V_{DS,p}^2\right] \tag{5.58}$$

Using equations (5.51) and (5.52), this expression can be rewritten as

$$\frac{k_n}{2}\cdot\left(V_{in} - V_{T0,n}\right)^2 = \frac{k_p}{2}\cdot\left[2\cdot\left(V_{in} - V_{DD} - V_{T0,p}\right)\cdot\left(V_{out} - V_{DD}\right) - \left(V_{out} - V_{DD}\right)^2\right] \tag{5.59}$$

To satisfy the derivative condition at V_{IL}, we differentiate both sides of (5.59) with respect to V_{in}.

$$k_n\cdot\left(V_{in} - V_{T0,n}\right) = k_p\cdot\left[\left(V_{in} - V_{DD} - V_{T0,p}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right) + \left(V_{out} - V_{DD}\right) - \left(V_{out} - V_{DD}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)\right] \tag{5.60}$$

Substituting $V_{in} = V_{IL}$ and $(dV_{out}/dV_{in}) = -1$ in (5.60), we obtain

$$k_n \cdot \left(V_{IL} - V_{T0,n}\right) = k_p \cdot \left(2\,V_{out} - V_{IL} + V_{T0,p} - V_{DD}\right) \tag{5.61}$$

The critical voltage V_{IL} can now be found as a function of the output voltage V_{out}, as follows:

$$V_{IL} = \frac{2\,V_{out} + V_{T0,p} - V_{DD} + k_R\,V_{T0,n}}{1 + k_R} \tag{5.62}$$

where k_R is defined as

$$k_R = \frac{k_n}{k_p}$$

This equation must be solved together with the KCL equation (5.59) to obtain the numerical value of V_{IL} and the corresponding output voltage, V_{out}. Note that the solution is fairly straightforward and does not require numerical iterations as in the previous cases, since none of the transistors is subject to substrate-bias effects.

Calculation of V_{IH}

When the input voltage is equal to V_{IH}, the nMOS transistor operates in the linear region, and the pMOS transistor operates in saturation. Applying KCL to the output node, we obtain

$$\frac{k_n}{2} \cdot \left[2 \cdot \left(V_{GS,n} - V_{T0,n}\right) \cdot V_{DS,n} - {V_{DS,n}}^2\right] = \frac{k_p}{2} \cdot \left(V_{GS,p} - V_{T0,p}\right)^2 \tag{5.63}$$

Using equations (5.51) and (5.52), this expression can be rewritten as

$$\frac{k_n}{2} \cdot \left[2 \cdot \left(V_{in} - V_{T0,n}\right) \cdot V_{out} - {V_{out}}^2\right] = \frac{k_p}{2} \cdot \left(V_{in} - V_{DD} - V_{T0,p}\right)^2 \tag{5.64}$$

Now, differentiate both sides of (5.64) with respect to V_{in}:

$$k_n \cdot \left[\left(V_{in} - V_{T0,n}\right) \cdot \left(\frac{dV_{out}}{dV_{in}}\right) + V_{out} - V_{out} \cdot \left(\frac{dV_{out}}{dV_{in}}\right)\right] = k_p \cdot \left(V_{in} - V_{DD} - V_{T0,p}\right) \tag{5.65}$$

Substituting $V_{in} = V_{IH}$ and $(dV_{out}/dV_{in}) = -1$ in (5.65), we obtain

$$k_n \cdot \left(-V_{IH} + V_{T0,n} + 2V_{out}\right) = k_p \cdot \left(V_{IH} - V_{DD} - V_{T0,p}\right) \tag{5.66}$$

The critical voltage V_{IH} can now be found as a function of V_{out} as follows:

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R \cdot \left(2V_{out} + V_{T0,n}\right)}{1 + k_R} \tag{5.67}$$

Again, this equation must be solved simultaneously with the KCL equation (5.64) to obtain the numerical values of V_{IH} and V_{out}.

Calculation of V_{th}

The inverter threshold voltage is defined as $V_{th} = V_{in} = V_{out}$. Since the CMOS inverter exhibits large noise margins and a very sharp VTC transition, the inverter threshold voltage emerges as an important parameter characterizing the DC performance of the inverter. For $V_{in} = V_{out}$, both transistors are expected to be in saturation mode; hence, we can write the following KCL equation.

$$\frac{k_n}{2} \cdot \left(V_{GS,n} - V_{T0,n}\right)^2 = \frac{k_p}{2} \cdot \left(V_{GS,p} - V_{T0,p}\right)^2 \tag{5.68}$$

Replacing $V_{GS,n}$ and $V_{GS,p}$ in (5.68) according to (5.51) and (5.52), we obtain

$$\frac{k_n}{2} \cdot \left(V_{in} - V_{T0,n}\right)^2 = \frac{k_p}{2} \cdot \left(V_{in} - V_{DD} - V_{T0,p}\right)^2 \tag{5.69}$$

The correct solution for V_{in} for this equation is

$$V_{in} \cdot \left(1 + \sqrt{\frac{k_p}{k_n}}\right) = V_{T0,n} + \sqrt{\frac{k_p}{k_n}} \cdot \left(V_{DD} + V_{T0,p}\right) \tag{5.70}$$

Finally, the inverter threshold (switching threshold) voltage V_{th} is found as

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot \left(V_{DD} + V_{T0,p}\right)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)} \tag{5.71}$$

Note that the inverter threshold voltage is defined as $V_{th} = V_{in} = V_{out}$. When the input voltage is equal to V_{th}, however, we find that the output voltage can actually attain any value between $(V_{th} - V_{T0,n})$ and $(V_{th} - V_{T0,p})$, without violating the voltage conditions used in this analysis. This is due to the fact that the VTC segment corresponding to Region C in Fig. 5.17 becomes completely vertical if the channel-length modulation effect is neglected, i.e., if $\lambda = 0$. In more realistic cases with $\lambda > 0$, the VTC segment in Region C exhibits a finite, but very large, slope. Figure 5.22 shows the variation of the inversion (switching) threshold voltage V_{th} as a function of the transconductance ratio k_R, and for fixed values of V_{DD}, $V_{T0,n}$ and $V_{T0,p}$.

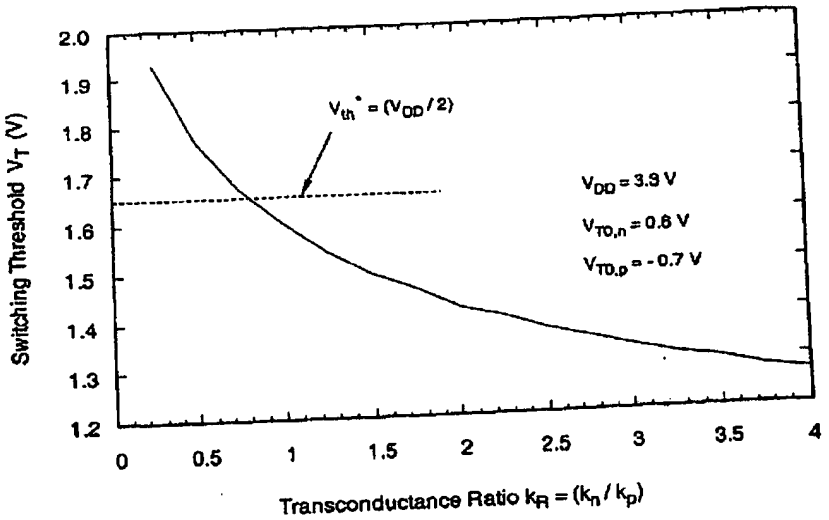


Figure 5.22. Variation of the inversion threshold voltage as a function of k_R.

It has already been established that the CMOS inverter does not draw any significant current from the power source, except for small leakage and subthreshold currents, when the input voltage is either smaller than $V_{T0,n}$ or larger than $(V_{DD}+V_{T0,p})$. The nMOS and the pMOS transistors conduct a nonzero current, on the other hand, during low-to-high and high-to-low transitions, i.e., in Regions B, C, and D. It can be shown that the current being drawn from the power source during transition reaches its peak value when $V_{in} = V_{th}$. In other words, the maximum current is drawn when both transistors are operating in saturation mode. Figure 5.23 shows the voltage transfer characteristic of a typical CMOS inverter circuit and the power supply current, as a function of the input voltage.

Design of CMOS Inverters

The inverter threshold voltage V_{th} was identified as one of the most important parameters that characterize the steady-state input-output behavior of the CMOS inverter circuit. The

CMOS inverter can, by virtue of its complementary push-pull operating mode, provide a full output voltage swing between 0 and V_{DD}, and therefore, the noise margins are relatively wide. Thus, the problem of designing a CMOS inverter can be reduced to setting the inverter threshold to a desired voltage value.

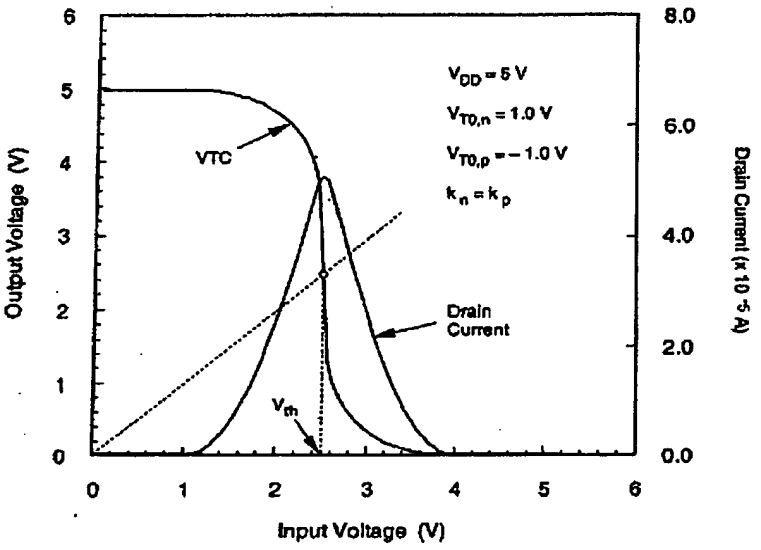


Figure 5.23. Typical VTC and the power supply current of a CMOS inverter circuit.

Given the power supply voltage V_{DD}, the nMOS and the pMOS transistor threshold voltages, and the desired inverter threshold voltage V_{th}, the corresponding ratio k_R can be found as follows. Reorganizing (5.71) yields

$$\sqrt{\frac{1}{k_R}} = \frac{V_{th} - V_{T0,n}}{V_{DD} + V_{T0,p} - V_{th}} \tag{5.72}$$

Now solve for k_R that is required to achieve the given V_{th}.

$$k_R = \frac{k_n}{k_p} = \left(\frac{V_{DD} + V_{T0,p} - V_{th}}{V_{th} - V_{T0,n}} \right)^2 \tag{5.73}$$

Recall that the switching threshold voltage of an *ideal* inverter is defined as

$$V_{th,ideal} = \frac{1}{2} \cdot V_{DD} \tag{5.74}$$

Substituting (5.74) in (5.73) gives

$$\left(\frac{k_n}{k_p}\right)_{ideal} = \left(\frac{0.5\,V_{DD} + V_{T0,p}}{0.5\,V_{DD} - V_{T0,n}}\right)^2 \tag{5.75}$$

for a near-ideal CMOS VTC that satisfies the condition (5.74). Since the operations of the nMOS and the pMOS transistors of the CMOS inverter are fully complementary, we can achieve completely symmetric input-output characteristics by setting the threshold voltages as $V_{T0} = V_{T0,n} = |V_{T0,p}|$. This reduces (5.75) to:

$$\left(\frac{k_n}{k_p}\right)_{\substack{symmetric\\inverter}} = 1 \tag{5.76}$$

Note that the ratio k_R is defined as

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \cdot \left(\frac{W}{L}\right)_p} = \frac{\mu_n \cdot \left(\frac{W}{L}\right)_n}{\mu_p \cdot \left(\frac{W}{L}\right)_p} \tag{5.77}$$

assuming that the gate oxide thickness t_{ox}, and hence, the gate oxide capacitance C_{ox} have the same value for both nMOS and pMOS transistors. The unity-ratio condition (5.76) for the ideal symmetric inverter requires that

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230\ \text{cm}^2/\text{V}\cdot\text{s}}{580\ \text{cm}^2/\text{V}\cdot\text{s}} \tag{5.78}$$

Hence,

$$\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n \tag{5.79}$$

It should be noted that the numerical values used in (5.78) for electron and hole mobilities are *typical* values, and that exact μ_n and μ_p values will vary with surface doping concentration of the substrate and the tub. The VTCs of three CMOS inverter circuits with different k_R ratios are shown in Fig. 5.24. It can be seen clearly that the inverter threshold voltage V_{th} shifts to lower values with increasing k_R ratio.

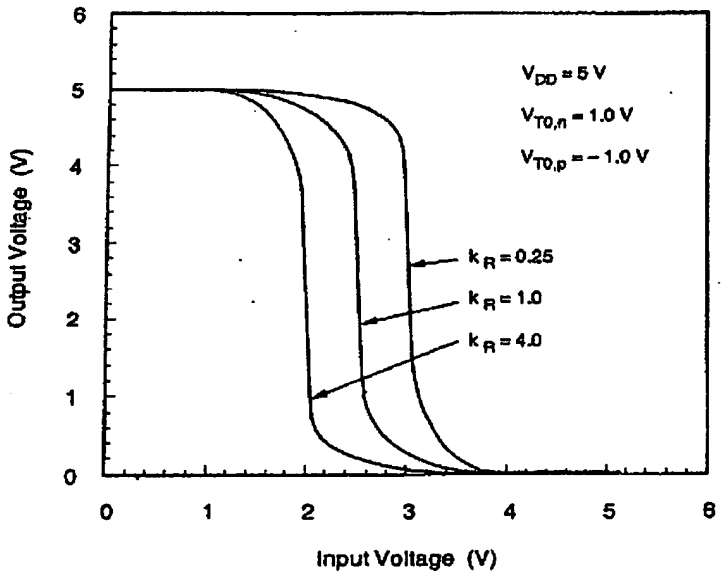


Figure 5.24. Voltage transfer characteristics of three CMOS inverters, with different nMOS-to-pMOS ratios.

For a symmetric CMOS inverter with $V_{T0,n} = |V_{T0,p}|$ and $k_R = 1$, the critical voltage V_{IL} can be found, using (5.62), as follows:

$$V_{IL} = \frac{1}{8} \cdot \left(3 V_{DD} + 2 V_{T0,n}\right) \tag{5.80}$$

Also, the critical voltage V_{IH} is found as

$$V_{IH} = \frac{1}{8} \cdot \left(5 V_{DD} - 2 V_{T0,n}\right) \tag{5.81}$$

Note that the sum of V_{IL} and V_{IH} is always equal to V_{DD} in a symmetric inverter.

$$V_{IL} + V_{IH} = V_{DD} \tag{5.82}$$

The noise margins NM_L and NM_H for this symmetric CMOS inverter are now calculated using (5.3) and (5.4).

$$NM_L = V_{IL} - V_{OL} = V_{IL}$$
$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} \tag{5.83}$$

which are equal to each other, and also to V_{IL}.

$$NM_L = NM_H = V_{IL} \tag{5.84}$$

Example 5.4

Consider a CMOS inverter circuit with the following parameters :

$V_{DD} = 3.3$ V
$V_{T0,n} = 0.6$ V
$V_{T0,p} = -0.7$ V
$k_n = 200\ \mu A/V^2$
$k_p = 80\ \mu A/V^2$

Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has $k_R = 2.5$ and $V_{T0,n} \neq |V_{T0,p}|$; hence, it is not a symmetric inverter.

First, the output low voltage V_{OL} and the output high voltage V_{OH} are found, using (5.54) and (5.55), as $V_{OL} = 0$ and $V_{OH} = 5$ V. To calculate V_{IL} in terms of the output voltage, we use (5.62).

$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R}$$
$$= \frac{2V_{out} - 0.7 - 3.3 + 1.5}{1 + 2.5} = 0.57 V_{out} - 0.71$$

Now substitute this expression into the KCL equation (5.59).

$$2.5(0.57V_{out} - 0.71 - 0.6)^2 = 2(0.57V_{out} - 0.71 - 3.3 + 0.7)(V_{out} - 3.3) - (V_{out} - 3.3)^2$$

This expression yields a second-order polynomial in V_{out}, as follows:

$$0.66 V_{out}^2 + 0.05 V_{out} - 6.65 = 0$$

Only one root of this quadratic equation corresponds to a physically correct solution for V_{out} (i.e., $V_{out} > 0$).

$$V_{out} = 3.14 \text{ V}$$

From this value, we can calculate the critical voltage V_{IL} as:

$$V_{IL} = 0.57 \cdot 3.14 - 0.71 = \underline{1.08 \text{ V}}$$

To calculate V_{IH} in terms of the output voltage, use (5.67):

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R \cdot \left(2V_{out} + V_{T0,n}\right)}{1 + k_R}$$
$$= \frac{3.3 - 0.7 + 2.5\left(2V_{out} + 0.6\right)}{1 + 2.5} = 1.43 V_{out} + 1.17$$

Next, substitute this expression into the KCL equation (5.64) to obtain a second-order polynomial in V_{out}.

$$2.5\left[2\left(1.43 V_{out} + 1.17 - 0.6\right)V_{out} - V_{out}^2\right] = \left(1.43 V_{out} - 1.43\right)^2$$

$$2.61 V_{out}^2 + 6.94 V_{out} - 2.04 = 0$$

Again, only one root of this quadratic equation corresponds to the physically correct solution for V_{out} at this operating point, i.e., when $V_{in} = V_{IH}$.

$$V_{out} = 0.27 \text{ V}$$

From this value, we can calculate the critical voltage V_{IH} as:

$$V_{IH} = 1.43 \cdot 0.37 + 1.17 = \underline{1.55 \text{ V}}$$

Finally, we find the noise margins for low voltage levels and for high voltage levels using (5.3) and (5.4).

$$NM_L = V_{IL} - V_{OL} = 1.08 \text{ V}$$
$$NM_H = V_{OH} - V_{IH} = 1.75 \text{ V}$$

Supply Voltage Scaling in CMOS Inverters

In the following, we will briefly examine the effects of supply voltage scaling, i.e., reduction of V_{DD}, upon the static voltage transfer characteristics of CMOS inverters. The

overall power dissipation of any digital circuit is a strong function of the supply voltage V_{DD}. With the growing trend for reducing the power dissipation in large-scale integrated systems and especially in portable applications, reduction (or scaling) of the power supply voltage emerges as one of the most widely practiced measures for low-power design. While such reduction is usually very effective, several important issues must also be addressed so that the system performance is not sacrificed. In this context, it is quite relevant to explore the influence of supply voltage scaling upon the VTC of simple CMOS inverter circuits.

The expressions we have developed in this section for V_{IL}, V_{IH}, and V_{th} indeed show that the static characteristics of the CMOS inverter allow significant variation of the supply voltage without affecting the functionality of the basic inverter. Neglecting second-order effects such as subthreshold conduction, it can be seen that the CMOS inverter will continue to operate correctly with a supply voltage which is as low as the following limit value.

$$V_{DD}^{min} = V_{T0,n} + |V_{T0,p}| \tag{5.85}$$

This means that correct inverter operation will be sustained if at least one of the transistors remains in conduction, for any given input voltage. Figure 5.25 shows the voltage transfer characteristics of a CMOS inverter, obtained with different supply voltage levels. The exact shape of the VTC near the limit value is essentially determined by subthreshold conduction properties of the nMOS and pMOS transistors, yet it is clear that the circuit operates as an inverter over a large range of supply voltages levels.

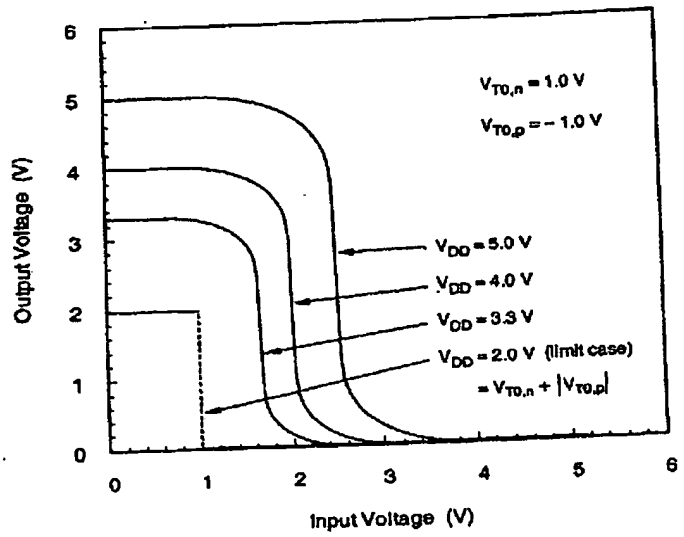


Figure 5.25. Voltage transfer characteristics of a CMOS inverter, obtained with different power supply voltage levels.

It is interesting to note that the CMOS inverter will continue to operate, albeit somewhat differently, even beyond the limit described in (5.85). If the power supply voltage is reduced *below* the sum of the two threshold voltages, the VTC will contain a region in which none of the transistors is conductiong. The output voltage level within this region is then determined by the *previous state* of the output, since the previous output level is always preserved as stored charge at the output node. Thus, the VTC exhibits a *hysteresis* behavior for very low supply voltage levels, which is illustrated in Fig. 5.26.

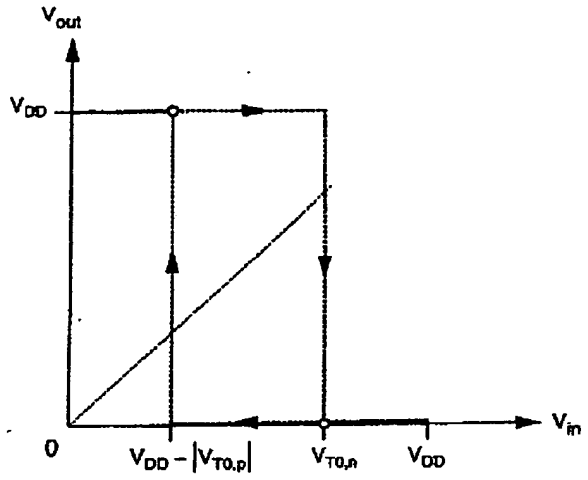


Figure 5.26. Voltage transfer characteristic of a CMOS inverter, operated with a supply voltage which is lower than the limit given in (5.85).

Power and Area Considerations

Since the CMOS inverter does not draw any significant current from the power source in both of its steady-state operating points ($V_{out} = V_{OH}$ and $V_{out} = V_{OL}$), the DC power dissipation of this circuit is almost negligible. The drain current that flows through the nMOS and the pMOS transistors in both cases is essentially limited to the reverse leakage current of the source and drain pn-junctions, and in short-channel MOSFETs, the relatively small subthreshold current. This unique property of the CMOS inverter was already identified as one of the most important advantages of this configuration. In many applications requiring a low overall power consumption, CMOS is preferred over other circuit alternatives for this reason. It must be noted, however, that the CMOS inverter does conduct a significant amount of current during a *switching event*, i.e., when the output voltage changes from a low to high state, or from a high to low state. The detailed calculation of this *dynamic power dissipation* will be examined in Chapters 6 and 11.

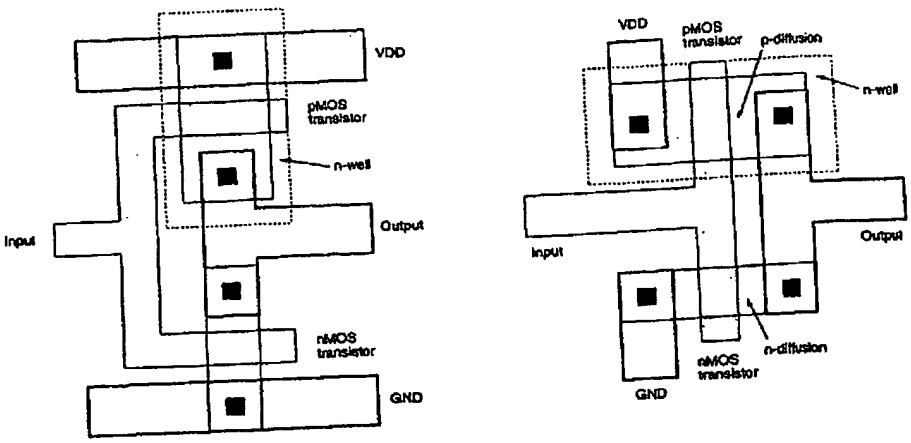


Figure 5.27. Two sample layouts of CMOS inverter circuits (for p-type substrate).

Figure 5.27 shows two layout examples for the simple CMOS inverter circuit. In both cases, it is assumed that the circuit is being built on a *p*-type wafer, which also provides the substrate for the nMOS transistor. The pMOS transistor, on the other hand, must be placed in an n-well (dotted lines), which becomes the substrate for this device. Also note that in Fig. 5.27 the channel width of the pMOS transistor is larger than that of the nMOS transistor. This is typical for symmetric inverter configurations, in which the k_R ratio is set approximately equal to unity.

Compared to other inverter layouts examined in previous sections, the CMOS inverters shown in Fig. 5.27 do not occupy significantly more area. The added complexity of the fabrication process (creating n-well diffusion, separate p-type and n-type source and drain diffusions, etc.) appears to be the only drawback for the inverter example. Because of the complementary nature of this circuit configuration, however, CMOS random logic circuits require significantly more transistors for the same function than their nMOS counterparts. Consequently, CMOS logic circuits tend to occupy more area than comparable nMOS logic circuits, which apparently affects the integration density of pure-CMOS logic. The actual integration density of nMOS logic, on the other hand, is limited by power dissipation and heat generation problems.

References

1. N.H.E. Weste and K. Eshraghian, *Principles of CMOS VLSI Design–A Systems Perspective*, second edition, Reading, MA: Addison-Wesley, 1993.

2. J.P. Uyemura, *Fundamentals of MOS Digital Integrated Circuits*, Reading, MA: Addison-Wesley, 1988.

It can be seen that the propagation delay of the lumped RC network is about 2.5 ns (regardless of signal flow direction), while the propagation delay of the 10-segment RC ladder network is about 0.7 ns (for signal flow from B to A). In this case, the difference between the delay times is significantly more pronounced due to the nonuniform distribution of parasitics. As in the previous example, we also construct the simple T-model of this nonuniform interconnect line, consisting of one lumped capacitor (356 fF) and two lumped resistors (2.5 kΩ and 7.5 kΩ). The T-model again yields a significantly more accurate transient response, and it correctly represents the directional dependence of propagation delay times which is due to the nonuniform geometry of the line.

6.7. Switching Power Dissipation of CMOS Inverters

It was shown in Chapter 5 that the static power dissipation of the CMOS inverter is quite negligible. During switching events where the output load capacitance is alternatingly charged up and charged down, on the other hand, the CMOS inverter inevitably dissipates power. In the following section, we will derive the expressions for the dynamic power consumption of the CMOS inverter.

Consider the simple CMOS inverter circuit shown in Fig. 6.27. We will assume that the input voltage is an ideal step waveform with negligible rise and fall times. Typical input and output voltage waveforms and the expected load capacitor current waveform are shown in Fig. 6.28. When the input voltage switches from low to high, the pMOS transistor in the circuit is turned off, and the nMOS transistor starts conducting. During this phase, the output load capacitance C_{load} is being discharged through the nMOS transistor. Thus, the capacitor current equals the instantaneous drain current of the nMOS transistor. When the input voltage switches from high to low, the nMOS transistor in the circuit is turned off, and the pMOS transistor starts conducting. During this phase, the output load capacitance C_{load} is being charged up through the pMOS transistor; therefore, the capacitor current equals the instantaneous drain current of the pMOS transistor.

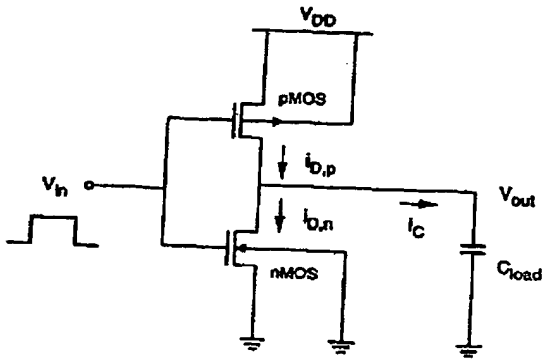


Figure 6.27. CMOS inverter used in the dynamic power-dissipation analysis.

Assuming periodic input and output waveforms, the average power dissipated by any device over one period can be found as follows:

$$P_{avg} = \frac{1}{T}\int_0^T v(t)\cdot i(t)\,dt \tag{6.66}$$

Since during switching, the nMOS transistor and the pMOS transistor in a CMOS inverter conduct current for one-half period each, the average power dissipation of the CMOS inverter can be calculated as the power required to charge up and charge down the output load capacitance.

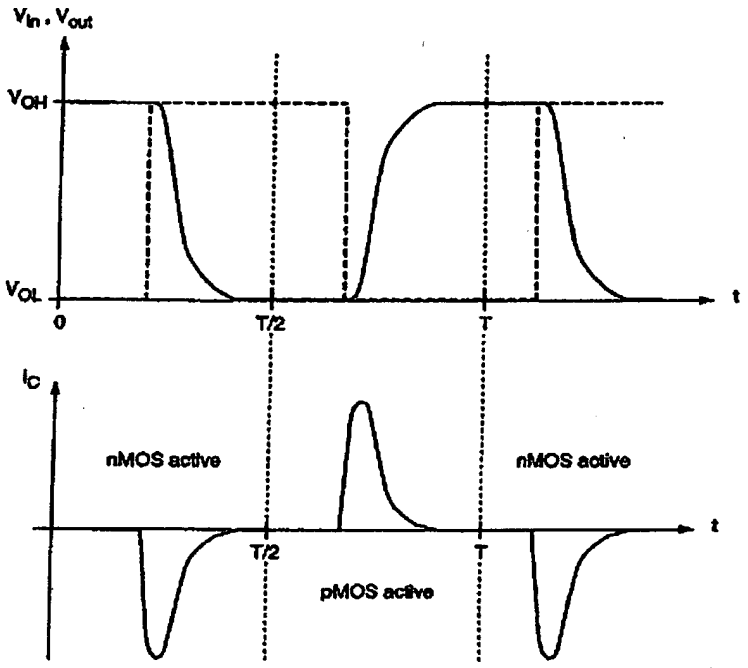


Figure 6.28. Typical input and output voltage waveforms and the capacitor current waveform during switching of the CMOS inverter.

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}(V_{DD}-V_{out})\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right] \tag{6.67}$$

Evaluating the integrals in (6.67), we obtain

$$P_{avg} = \frac{1}{T}\left[\left(-C_{load}\frac{V_{out}^2}{2}\right)\Big|_0^{T/2} + \left(V_{DD}\cdot V_{out}\cdot C_{load} - \frac{1}{2}C_{load}V_{out}^2\right)\Big|_{T/2}^{T}\right] \tag{6.68}$$

$$P_{avg} = \frac{1}{T}C_{load}V_{DD}^2 \tag{6.69}$$

Noting that $f = 1/T$, this expression can also be written as:

$$P_{avg} = C_{load}\cdot V_{DD}^2 \cdot f \tag{6.70}$$

It is clear that the average power dissipation of the CMOS inverter is proportional to the switching frequency f. Therefore, the low-power advantage of CMOS circuits becomes less prominent in high-speed operation, where the switching frequency is high. Also note that the average power dissipation is independent of all transistor characteristics and transistor sizes. Consequently, the switching delay times have no relevance to the amount of power consumption during the switching events. The reason for this is that the switching power is solely dissipated for charging and discharging the output capacitance from V_{OL} to V_{OH}, and vice versa.

For this reason, the switching power expression derived for the CMOS inverter also applies to all general CMOS circuits, as shown in Fig. 6.29. A general CMOS logic circuit

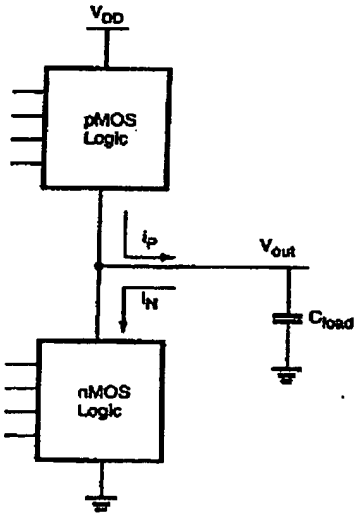


Figure 6.29. Generalized CMOS logic circuit.

consists of an nMOS logic block between the output node and the ground, and a pMOS logic block between the output and V_{DD}. As in the simple CMOS inverter case, either the pMOS block *or* the nMOS block can conduct depending on the input voltage combination, but not both at the same time. Therefore, switching power is again dissipated solely for charging and discharging the output capacitance.

To summarize, if the total parasitic capacitance in the circuit can be lumped at the output node with reasonable accuracy, if the output voltage swing is between 0 and V_{DD}, and if the input voltage waveforms are assumed to be ideal step inputs, the average switching power expression (6.70) will hold for any CMOS logic circuit.

Note that under realistic conditions, when the input voltage waveform deviates from ideal step input and has nonzero rise and fall times, for example, both the nMOS and the pMOS transistor will simultaneously conduct a certain amount of current during the switching event. This is called the short-circuit current, since in this case, the two transistors temporarily form a conducting path between the V_{DD} and the ground. The additional power dissipation, which is due to the short-circuit current, cannot be predicted by the power-dissipation formula (6.70) derived above, since the short-circuit current is not being utilized to charge or discharge the output load capacitor. We must be aware that this additional power-dissipation term can be quite significant under some nonideal conditions. If the load capacitance is increased, on the other hand, the short-circuit dissipation term usually becomes negligible in comparison to the power dissipation which is due to the charging/discharging of capacitances.

Power Meter Simulation

In the following, we present a simple circuit simulation approach which can be used to estimate the average power dissipation of arbitrary circuits (including the effects of short circuit and leakage currents), under realistic operating conditions. According to (6.66), the average power dissipation of any device or circuit which is driven by a periodic input waveform can be found by integrating the product of its instantaneous terminal voltage and its instantaneous terminal current over one period. If we have to determine the amount of P_{avg} drawn from the power supply over one period, the problem is reduced to finding only the time-average of the power supply current, since the power supply voltage is a constant.

Using a simple simulation model called the *power meter*, we can estimate the average power dissipation of an arbitrary device or circuit driven by a periodic input, with transient circuit simulation. Consider the circuit structure shown in Fig. 6.30, in which a zero-volt independent voltage source is connected in series with the power supply voltage source V_{DD} of the device or circuit in question. Consequently, the instantaneous power supply current $i_{DD}(t)$ which is being drawn by the circuit will also pass through the zero-volt voltage source, $i_s(t) = i_{DD}(t)$.

The power meter circuit consists of three elements: a linear current-controlled current source, a capacitor, and a resistor, all connected in parallel. The current equation for the common node of the power meter circuit can be written as follows:

$$C_y \frac{dV_y}{dt} = \beta i_s - \frac{V_y}{R_y} \tag{6.71}$$

where C_i represents the parasitic capacitance associated with each node in the circuit (including the output node) and α_{Ti} represents the corresponding node transition factor associated with that node. Hence, the terms in the parentheses in (11.5) represent the total amount of *charge* which is drawn from the power supply during each switching event. While (11.5) is a more exact representation of the switching power dissipation in a CMOS logic gate, its evaluation may be relatively complicated. Therefore, we will mainly rely on (11.4) to express the switching power dissipation in CMOS logic circuits.

Observations on Switching Power Reduction

Expressions (11.4) and (11.5) derived above for the average switching power dissipation of CMOS logic gates suggest that we have several different means for reducing the power consumption. These measures include (i) reduction of the power supply voltage V_{DD}, (ii) reduction of the voltage swing in all nodes, (iii) reduction of the switching probability (transition factor) and (iv) reduction of the load capacitance. Note that the switching power dissipation is also a linear function of the clock frequency, yet simply reducing the frequency would significantly diminish the overall system performance. Thus, the reduction of clock frequency would be a viable option only in cases where the overall throughput of the system can be maintained by other means.

The reduction of power supply voltage is one of the most widely practiced measures for low-power design. While such reduction is usually very effective, several important issues must be addressed so that the system performance is not sacrificed. In particular, we need to consider that reducing the power supply voltage leads to an increase of delay. Also, the input and output signal levels of a low-voltage circuit or module should be made compatible with the peripheral circuitry, in order to maintain correct signal transmission.

The reduction of switching activity requires a detailed analysis of signal transition probabilities, and implementation of various circuit-level and system-level measures such as logic optimization, use of gated clock signals and prevention of glitches. Finally, the load capacitance can be reduced by using certain circuit design styles and by proper transistor sizing. These and other methods for the reduction of switching power dissipation will be examined in detail in the following Sections.

Short-Circuit Power Dissipation

The switching power dissipation examined above is purely due to the energy required to charge up the parasitic load capacitances in the circuit, and the switching power is independent of the rise and fall times of the input signals. Yet, if a CMOS inverter (or a logic gate) is driven with input voltage waveforms with finite rise and fall times, both the nMOS and the pMOS transistors in the circuit may conduct *simultaneously* for a short amount of time during switching, forming a direct current path between the power supply and the ground, as shown in Fig. 11.4.

The current component which passes through both the nMOS and the pMOS devices during switching does not contribute to the charging of the capacitances in the circuit, and hence, it is called the *short-circuit current* component. This component is especially prevalent if the output load capacitance is small, and/or if the input signal rise and fall times are large, as seen in Fig. 11.5. Here, the input/output voltage waveforms and the components of the current drawn from the power supply are illustrated for a symmetrical

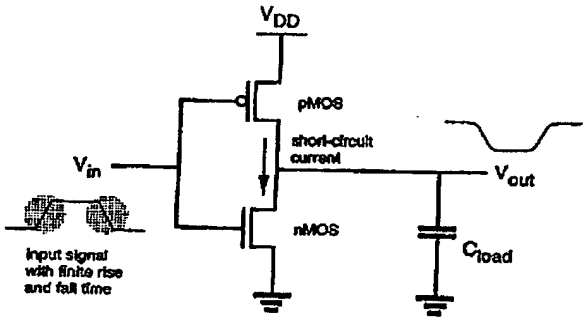


Figure 11.4. Both nMOS and pMOS transistor may conduct (simultaneously) a short-circuit current during switching.

CMOS inverter with small capacitive load. The nMOS transistor in the circuit starts conducting when the rising input voltage exceeds the threshold voltage $V_{T,n}$. The pMOS transistor remains on until the input reaches the voltage level ($V_{DD} - |V_{T,p}|$). Thus, there is a time window during which both transistors are turned on. As the output capacitance is discharged through the nMOS transistor, the output voltage starts to fall. The drain-to-source voltage drop of the pMOS transistor becomes nonzero, which allows the pMOS transistor to conduct as well. The short circuit current is terminated when the input voltage transition is completed and the pMOS transistor is turned off. A similar event is responsible for the short-circuit current component during the falling input transition, when the output voltage starts rising while both transistors are on.

Note that the magnitude of the short-circuit current component will be approximately the same during both the rising-input transition and the falling-input transition, assuming that the inverter is symmetrical and the input rise and fall times are identical. The pMOS transistor also conducts the current which is needed to charge up the small output load capacitance, but only during the falling-input transition (the output capacitance is discharged through the nMOS device during the rising-input transition). This current component, which is responsible for the switching power dissipation of the circuit (current component to charge up the load capacitance), is also shown in Fig. 11.5. The average of both of these current components determines the total amount of power drawn from the supply.

For a simple analysis consider a symmetric CMOS inverter with $k_n = k_p = k$ and $V_{T,n} = |V_{T,p}| = V_T$, and with a very small capacitive load. If the inverter is driven with an input voltage waveform with equal rise and fall times ($\tau_{rise} = \tau_{fall} = \tau$), it can be derived that the time-averaged short circuit current drawn from the power supply is

$$I_{avg}(short-circuit) = \frac{1}{12} \cdot \frac{k \cdot \tau \cdot f_{CLK}}{V_{DD}} (V_{DD} - 2V_T)^3 \qquad (11.6)$$

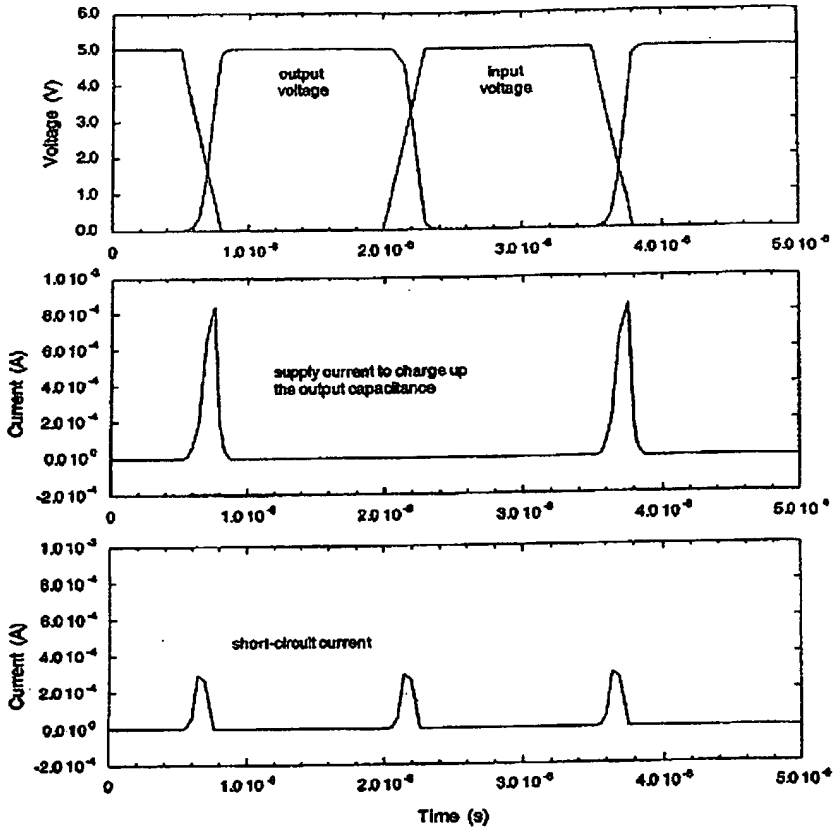


Figure 11.5. Input-output voltage waveforms, the supply current used to charge up the capacitance and the short-circuit current in a CMOS inverter with small capacitive load. The current drawn from the power supply is the sum of both current components.

Hence, the short-circuit power dissipation becomes

$$P_{avg}(short-circuit) = \frac{1}{12} \cdot k \cdot \tau \cdot f_{CLK} \cdot (V_{DD} - 2V_T)^3$$

Note that the short-circuit power dissipation is linearly proportional to the input rise and fall times, and also to the transconductance of the transistors. Hence, the input transition times will decrease the short-circuit current component.

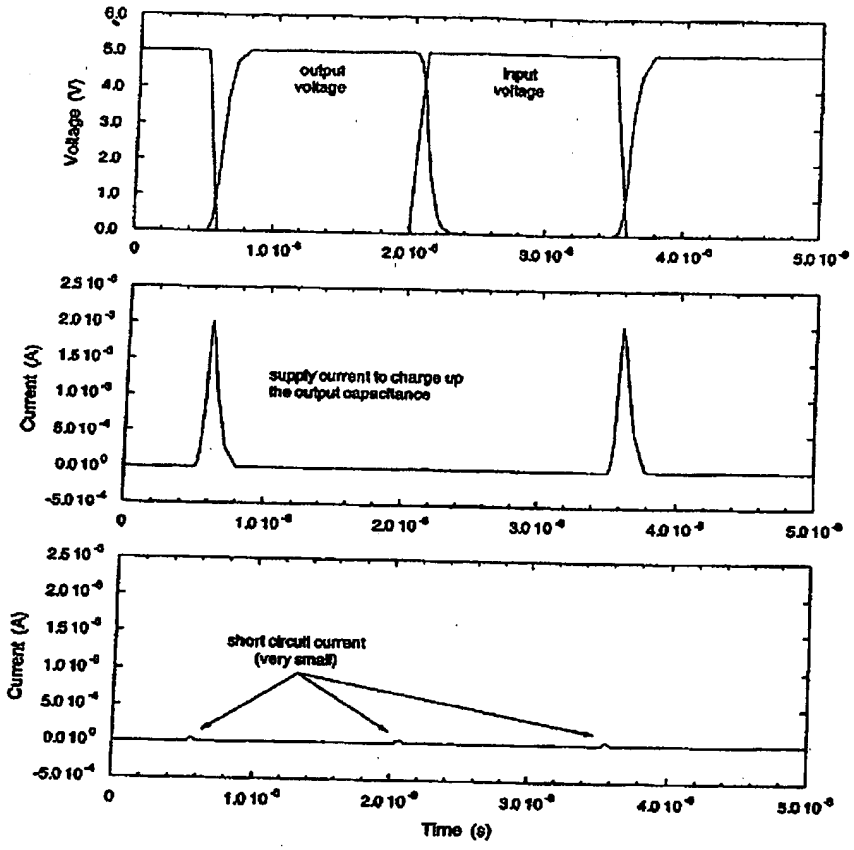


Figure 11.6. Input-output voltage waveforms, the supply current used to charge up the load capacitance and the short-circuit current in a CMOS inverter with larger capacitive load and smaller input transition times. The total current drawn from the power supply is approximately equal to the charge-up current.

Now consider the same CMOS inverter with a larger output load capacitance and smaller input transition times. During the rising input transition, the output voltage will effectively remain at V_{DD} until the input voltage completes its swing and the output will start to drop only after the input has reached its final value. Although both nMOS and pMOS transistors are on simultaneously during the transition, the pMOS transistor cannot conduct a significant amount of current since the voltage drop between its source and drain terminals is almost zero. Similarly, the output voltage will remain at approxi-

mately 0 V during the falling input transition and it will start to rise only after the input voltage completes its swing. Again, both transistors will be on simultaneously during the input voltage transition, yet the nMOS transistor will not be able to conduct a significant amount of current since its drain-to-source voltage is approximately zero. This situation is illustrated in Fig. 11.6, which shows the simulated input and output voltage waveforms of the inverter as well as the short-circuit and dynamic current components drawn from the power supply. Notice that the peak value of the supply current to charge up the output load capacitance is larger in this case. The reason for this is that the pMOS transistor remains in saturation during the entire input transition, as opposed to the previous case shown in Fig. 11.5 where the transistor leaves the saturation region before the input transition is completed.

The discussion concerning the magnitude of the short-circuit current may suggest that the short-circuit power dissipation can be reduced by making the output voltage transition times larger and/or by making the input voltage transition times smaller. Yet this goal should be balanced carefully against other performance goals such as propagation delay, and the reduction of the short-circuit current should be considered as one of the many design requirements that must be satisfied by the designer.

Leakage Power Dissipation

The nMOS and pMOS transistors used in a CMOS logic gate generally have nonzero reverse leakage and subthreshold currents. In a CMOS VLSI chip containing a very large number of transistors, these currents can contribute to the overall power dissipation even when the transistors are not undergoing any switching event. The magnitude of these leakage currents is determined mainly by the processing parameters.

Of the two main leakage current components in a MOSFET, the reverse diode leakage occurs when the pn-junction between the drain and the bulk of the transistor is revers-biased. The reverse-biased drain junction then conducts a reverse saturation current which is drawn from the power supply. Consider a CMOS inverter with a high input voltage, where the nMOS transistor is turned on and the output node voltage is discharged to zero. Although the pMOS transistor is turned off, there will be a reverse potential difference of V_{DD} between its drain and the n-well, causing a diode leakage through the drain junction. The n-well region of the pMOS transistor is also reverse biased with V_{DD}, with respect to the p-type substrate. Therefore, another significant leakage current component exists because of the n-well junction (Fig. 11.7).

A similar situation can be observed when the input voltage is zero, and the output voltage is charged up to V_{DD} through the pMOS transistor. Then, the reverse potential difference between the nMOS drain region and the p-type substrate causes a reverse leakage current which is also drawn from the power supply (through the pMOS transistor).

The reverse leakage current of a pn-junction is expressed by

$$I_{reverse} = A \cdot J_S \left(e^{\frac{q V_{diode}}{kT}} - 1 \right) \qquad (11$$

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.